UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,284	01/21/2004	Hisanobu Azuma	03560.003423.	9833

5514 7590 05/27/2005

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,284	AZUMA, HISANOBU	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 7* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 3, 6 and 7 are rejected under 35 U.S.C. 103(a) as being obvious over Takeda et al., U.S. Patent 6,726,520 B2.

4. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter

disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2). Optimization within prior art conditions or through routine experimentation generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical.

5. Pertaining to claim 1,Takeda discloses a semiconductor process substantially as claimed. See **FIGS. 1-25**, where Takeda teaches the following limitations.

Takeda teaches a method for electrifying a plurality of electric conductors arranged on a substrate comprising the step of setting an average temperature difference during electrifying processing between a region S_o in that the plurality of electric conductors on the substrate are arranged and a region S_1 located on the periphery of the region S_o. However Takeda fails to teach the temperature at 15° C or more, wherein the substrate satisfies the relational expression:

$L_1/L_o > E\alpha\Delta T/\sigma th - 1$.

where L_o [m] : the width of the region S_o

L_1[m]: the width of the region S_1

ΔT[K]: the average temperature difference

E[Pa]: the Young's modulus of the substrate

α[/K]: the coefficient of linear thermal expansion of the substrate

σth[Pa]: the material constant of the substrate. In view of Takeda, it would have been obvious to one of ordinary skill in the art to incorporate the optimized parameters of the claimed formula to discover, by routine experimentation that the temperature as claimed to prevent cracking of the substrate due to the variation in temperature during processing.

6. Pertaining to claim 2, Takeda teaches a method for manufacturing an electron-source substrate comprising the steps of:

electrifying a plurality of electric conductors arranged on a substrate in a hermetic atmosphere so as to impart an electron-emission function to part of the electric

conductors; and

setting an average temperature difference during the electrifying processing between a region S_o in that the plurality of electric conductors on the substrate are arranged and a region S_I located on the periphery of the region S_o. However Takeda fails to teach the temperature at 15° C or more, wherein the substrate satisfies the relational expression:

$L_1/L_o > E\alpha\Delta T/\sigma th - 1$.

where L_o [m] : the width of the region S_o

L_1[m]: the width of the region S_I

ΔT[K]: the average temperature difference

E[Pa]: the Young's modulus of the substrate

α[/K]: the coefficient of linear thermal expansion of the substrate

σth[Pa]: the material constant of the substrate. In view of Takeda, it would have been obvious to one of ordinary skill in the art to incorporate the optimized parameters of the claimed formula to discover, by routine experimentation that the temperature as claimed to prevent cracking of the substrate due to the variation in temperature during processing.

7. Pertaining to claim 3, Takeda teaches a manufacturing method according to Claim 2, further comprising the step of cutting the substrate into desired sizes after the electrifying processing
(the Examiner takes the position that it is well known to dice a wafer having a plurality of devices).

8. Pertaining to claim 4, Takeda teaches a manufacturing method according to Claim 3, wherein the cutting step comprises making dust-proof for covering the region of the electric conductors and at least one of the steps of wheel-cutter cutting, dicing, and sandblast cutting (it is well known to manufacture semiconductor devices in at least a class 1000 clean room, and if sandblast cutting is to take place, due to health code requirements a dust proof covering is well known to be incorporated).

9. Pertaining to claim 6, Takeda teaches a manufacturing method according to Claim 2, wherein the electrifying step in the hermetic atmosphere comprises the steps of covering the region of the electric conductors on the substrate with a container, and exhausting and introducing gas after the covering step.

10. Pertaining to claim 7, Takeda teaches a manufacturing method according to Claim 2, wherein the electric conductors each comprise a pair of electrodes and a conductive film formed between the electrodes and the electrodes are electrically connected to wiring.

Objections

11. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC